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(54) Bonded wafer structure having a buried insulator layer.

(57) A wafer structure and a method of making the same, upon which semiconductor devices may be formed, comprises first and second wafers. The first wafer (20) comprises a first substrate (24) having a thin oxide layer (26a) formed on a bottom surface thereof; the said first substrate having a characteristic thermal expansion coefficient. The second wafer (22) comprises a second substrate (28) having an insulation layer (30) formed on a top surface thereof, the insulation layer having a characteristic thermal expansion coefficient substantially matched with the characteristic thermal expansion coefficient of the first substrate and further having a high thermal conductivity. The second wafer further comprises a thin oxide layer (26b) formed on a top surface of the insulation layer, wherein the first thin oxide layer of the first wafer is bonded to the second thin oxide layer of the second wafer, to form a typical bonded wafer structure (10) that can be advantageously used in the fabrication of high speed high density integrated circuits.

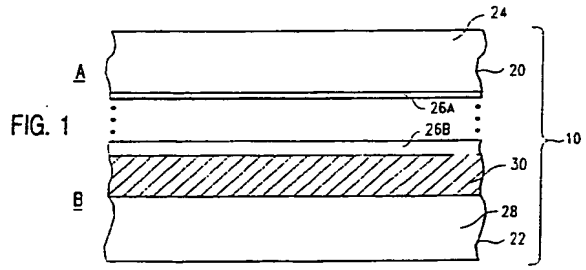

FIG. 1

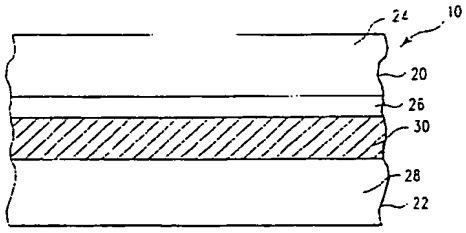

FIG. 2

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The present invention relates to wafer structures and a method of making the same. More particularly, the invention relates to a wafer structure containing an insulation layer.

Wafer structures having a "buried insulation" layer are particularly useful for semiconductor devices made via a BiCMOS process. The BiCMOS process is an integrated circuit processing technology which allows bipolar transistors to be formed within substrate wells containing complementary metal-oxide semiconductor (CMOS) transistors. An example of a BiCMOS semiconductor device is one in which "power-hungry" emitter coupled logic (ECL) bipolar circuits are used on a silicon-on-insulator (SOI) structure. The ECL circuits act as logic elements and bipolar drivers. One disadvantage of these ECL circuits is that they produce sufficient heat that the generated heat becomes trapped and gives rise to temperatures unacceptable for normal device operation.

In addition to temperature sensitivity, silicon devices are sensitive to radiation (e.g., _-radiation and cosmic radiation). In order to decrease the radiation sensitivity of the silicon device, the collection volume of the device has to be reduced for hole/electron pairs generated by the radiation impact along the radiation path. The collection volume can be reduced by incorporating a "buried insulation" layer in the silicon device structure.

Recently, the technology for forming "buried insulation" layers has advanced to the stage of manufacturing quantities. In particular, thermally grown SiO_2 is used as the buried insulation layer. Bonding two oxide grown wafers can be achieved at an elevated temperature (900 to 1100°C) whereby the two oxide layers become a single oxide layer. The excess silicon on the device wafer is then removed, first by grinding, then by lapping, and finally by chem.-mech. polishing. On the commercial market, 2µm thick silicon above a buried 5000Å thick SiO_2 oxide layer is obtainable, for example, from Shin-Etsu Handotai (S.E.H.) of Tokyo, Japan.

A buried isolation layer of thick thermal SiO_2 oxide (5000Å) can also be used for reducing heat build-up of the ECL circuits on an SOI structure, if a heat conducting path is provided. The use of thermally grown SiO_2, by itself, has disadvantages. For instance, the thermal resistance of the oxide is a function of thickness. The thermal resistance of the oxide layer can be minimized by making the layer thin, however, this would result in undesired increased capacitance effects. In addition, the thermal expansion coefficient of SiO_2 ($5X10^{-7}$ C^{-1}) is not well matched with the thermal expansion coefficient of silicon ($32X10^{-7}$ C^{-1}).

An alternative method for keeping a device cool is to incorporate a polycrystalline diamond layer within the semiconductor device structure as shown in US-A-4981818 entitled "Polycrystalline CVD Diamond Substrate For Single Crystal Epitaxial Growth Of Semiconductors" and granted Jan. 1, 1991 to Anthony et al.. In the '818 patent, a chemical vapor deposited (CVD) diamond layer is formed on a single crystal of silicon. During the deposition of the diamond layer, an intermediate layer of single crystal SiC forms between the single crystal of silicon and the polycrystalline CVD diamond layer. The silicon is then completely removed, via etching, to reveal the SiC layer supported on the polycrystalline CVD diamond layer. A semiconductor layer is thereafter epitaxially grown on the exposed single crystal of SiC. A single crystal semiconductor polycrystalline CVD diamond mounted device structure is thus produced.

A device produced via the teaching of the '818 patent, however, has disadvantages. For instance, the crystal quality of the semiconductor grown epitaxially on the SiC is subject to defects, such as, lattice mismatch. In addition, the CVD diamond layer becomes the support substrate for the semiconductor device, thus, necessitating a relatively thick CVD diamond layer. Furthermore, since the diamond substrate of the '818 patent is exposed, any subsequent device fabrication steps of high temperature, high energy processes in oxygen (such as oxidation, plasma ashing, etc.) will attack the substrate. Therefore, it is very difficult to perform process steps with the '818 diamond substrate for processes, such as, isolation trench formation, field isolation, and resist stripping.

It would thus be desirable to provide a wafer structure having a buried insulation layer which is free of the above identified problems. Such a structure should also provide a substrate which is substantially free of lattice mismatch defects and further provide optimal thermal dissipation. Still further, such a structure should be suitable for isolation trench formation.

According to the invention, a wafer structure having a buried insulation layer, upon which semiconductor structures may subsequently be formed, comprises first and second wafers. The first wafer comprises a first substrate having a thin oxide layer formed on a bottom surface thereof, the first substrate having a characteristic thermal expansion coefficient. The second wafer comprises a second substrate having an insulation layer formed on a top surface thereof, the insulation layer having a characteristic thermal expansion coefficient substantially matched with the characteristic thermal expansion coefficient of the first substrate and further having a high thermal conductivity. The second wafer further comprises a thin oxide layer formed on a top surface of the insulation layer. The first thin oxide layer of the first wafer is bonded to the second thin oxide layer of the second wafer.

Also, according to the present invention, a method of making a wafer structure having a buried insulation layer upon which semiconductor structures may subsequently be formed, comprises the steps of:

a) forming a first thin oxide layer on a bottom surface of a first substrate, the first substrate having a characteristic thermal expansion coefficient;

b) forming an insulation layer on a top surface of a second substrate, the insulation layer having a characteristic thermal expansion coefficient substantially matched with the characteristic thermal expansion coefficient of the first substrate and further having a high thermal conductivity;

c) forming a second thin oxide layer on a top surface of the insulation layer; and

d) bonding the first thin oxide layer to the second thin oxide layer.

The foregoing and other structures and teachings of the present invention will become more apparent upon a detailed description of the best mode for carrying out the invention as rendered below. In the description to follow, reference will be made to the accompanying drawings, in which:

FIG. 1a and 1b are cross-sectional views of a first wafer and a second wafer, respectively, at a processing step in accordance with a preferred embodiment of the present invention;

FIG. 2 is a cross-sectional view of the wafer structure according to the invention at a processing step subsequent to that shown by FIG. 1a. and 1b.;

FIG. 3 is a cross-sectional view of the wafer structure according to a preferred embodiment of the present invention;

FIG. 4a and 4b are cross-sectional views of a first wafer and a second wafer, respectively, at a processing step in accordance with an alternate embodiment of the present invention;

FIG. 5 is a cross-sectional view of the wafer structure according to the invention at a processing step subsequent to that shown by FIG. 4a. and 4b.;

FIG. 6 is a cross-sectional view of the wafer structure according to an alternate embodiment of the present invention;

FIG. 7 is a cross-sectional view of the wafer structure of the present invention at a processing step for isolation trench formation;

FIG. 8 is a cross-sectional view of the wafer structure of the present invention at a processing step subsequent to that shown by FIG. 7;

FIG. 9 is a cross-sectional view of the wafer structure of the present invention at a processing step subsequent to that shown by FIG. 8; and

FIG. 10 is a cross-sectional view of the wafer structure of the present invention at a processing step subsequent to that shown by FIG. 9.

Referring now to Figs. 1a and 1b, a bonded wafer structure 10 according to the present invention comprises a first primary wafer 20 and a secondary handle wafer 22. Primary wafer 20 comprises a substrate 24 having an oxide layer 26a formed on a bottom surface thereof. Substrate 24 preferably comprises an original silicon substrate having a thickness on the order of 100- 650μm. The original silicon substrate has a thermal expansion coefficient equal to approximately $32X10^{-7}$ C^{-1}. Additionally, the original silicon substrate has very low defect density. While substrate 24 has been described with reference to silicon, it should be known that, alternatively, substrate 24 can comprise an original germanium substrate.

Oxide layer 26a comprises a thin oxide layer having a thickness in the range of approximately 1-50 nm. Oxide layer 26a can be formed via conventional oxidation techniques whereby both top and bottom surfaces of substrate 24 can be oxidized or just one surface (only the bottom surface is discussed herein for simplicity). Preferably, oxide layer 26a comprises a silicon oxide layer of 250 nm in thickness, for instance, silicon dioxide (SiO_2), and is thermally grown in an oxygen ambient at approximately 800C°. Alternatively, oxide layer 26a. may comprise a pryolytically deposited, CVD oxide, or evaporate oxide, thus upon substrate 24, eliminating silicon consumption.

Secondary handle wafer 22 comprises a second substrate 28 having an insulation layer 30 formed on a top surface thereof. Substrate 28 preferably comprises an original silicon substrate having a thickness on the order of 100- 650μm. Substrate 28 may likewise comprise an original germanium substrate. On a top surface of substrate 28 is formed an insulation layer 30. Insulation layer 30 can comprise a diamond insulation layer having a thickness in the range of 0.01 to 1.0 μm. Preferably, insulation layer 30 is a chemical vapor deposited (CVD) diamond layer having a thickness of 0.5μm. CVD methods are well known in the art and therefore not discussed herein. CVD formation of diamond onto a substrate provides a slow deposition rate for providing a relatively uniform surface. The surface of the diamond layer does however contain bumps due to the crystal growth of the diamond. Diamond use is advantageous since diamond has a thermal coefficient of expansion equal to $18X10^{-7}$ C^{-1} which substantially matches and is similar to that of silicon ($32X10^{-7}$ C^{-1}). This is in comparison to that of silicon dioxide, which has a thermal coefficient of expansion equal to $5X10^{-7}$ C^{-1}. In addition, CVD diamond has a three orders of magnitude higher thermal conductivity (18-20 W/cm K) than thermally grown SiO_2, which has a low thermal conductivity (0.014 W/cm K). Furthermore, CVD diamond film has a dielectric constant between 3 and 6 (depending on the process) and a low dielectric resistivity between $1X10^{10}$ and $1X10^{16}$ ohm cm (depending on the process). It should be noted that insulation layer 30 could likewise comprise a diamond layer formed via plasma spray coating of diamond onto the top surface of substrate 28.

Referring still to Fig. 1b, an oxide layer 26b is formed on the top surface of insulation layer 30. Ox-

ide layer 26b performs a dual function. First, oxide layer 26b provides a buffer layer for overcoming the roughness of the top surface of insulation layer 30. Secondly, oxide layer 26b is used for bonding with oxide layer 26a. so as to bond primary wafer 20 to secondary handle wafer 22. In the preferred embodiment, insulation layer 30 comprises a diamond layer, whereby oxide layer 26b must be deposited onto the diamond layer instead of being thermally grown. Thermal oxidation of diamond film produces volatile material, resulting in the decomposition of the diamond film. Oxide layer 26b is also preferably comprised of a similar material as oxide layer 26a, i.e., a silicon oxide. Still further, oxide layer 26b is preferably pryolytically deposited SiO_2 having an initial thickness greater than 0.1 μm for overcoming the roughness of the diamond layer top surface. Oxide layer 26b is then subsequently planarized, for example, through any suitable known process of chem.-mech. polishing, to a thickness less than 0.1 μm. As a result, oxide layer 26b is relatively thin (i.e., < 0.1 μm or less than 20% in thickness) with respect to an insulation layer of SiO_2 having thickness of 0.5 μm as used in the prior art.

Primary wafer 20 is then placed in contact with secondary handle wafer 22 such that oxide layers 26a and 26b. are in intimate contact. Wafers 20 and 22 are then subjected to a heat treatment between 900 and 1100 °C for a period of time, for example two hours. As a result, the oxide layers 26a and 26b bond together, forming a single oxide layer 26 as shown in Fig. 2. The resultant single oxide layer 26 is still relatively thin, having a typical thickness in the range of 25-100 nm. In the preferred embodiment, oxide layer 26 comprises silicon dioxide and is approximately 500 Å in thickness.

The wafer structure 10 as shown in Fig. 2 can be further processed by a conventional sequence of grinding, lapping, wet etching, and chem.-mech. polishing to obtain wafer structure 10 as shown in Fig. 3. Grinding, lapping, wet etching, and chem.-mech. polishing are all well known in the art and further discussion thereof is not provided herein. Substrate 24 may be thinned to a desired thickness according to the requirements of a particular device. For instance, substrate 24 can be thinned to a thickness on the order of 2μm.

The resultant wafer structure 10 of Fig. 3 is thus suitable for the formation of semiconductor devices in the substrate 24. As described earlier, substrate 24 is preferably an original silicon substrate and is substantially free of lattice mismatch defects and other defects. Wafer structure 10 therefore provides a wafer structure having a buried insulation layer in combination with a substrate in which lattice mismatch defects are minimized. Additionally, the thermal expansion coefficient of the buried insulation layer is substantially matched to the thermal expansion coefficient of the substrate which provides highly efficient transfer of heat away from active semiconductor device areas. The insulation layer also has a high thermal conductivity. Still further, the presence of an insulation layer 30 comprising diamond film, in addition to the thin oxide layer 26, minimizes undesirable capacitive effects.

In an alternate embodiment according to the present invention (as shown in Figs. 4, 5, and 6), a wafer structure 100 is substantially similar to the preferred embodiment, with the following exceptions. A buffer layer 132, different from oxide layer 126b, is formed on a top surface of insulation layer 130 prior to the formation of oxide layer 126b. (see Fig. 4b). As previously noted, the surface of diamond film is rough and bumpy due the crystal structure of diamond. Buffer layer 132 is provided to overcome the roughness of the top surface of insulation layer 130 comprising diamond film. In particular, buffer layer 132 provides a relatively soft layer which can be planarized and which also facilitates oxide growth for subsequent bonding. Preferably, buffer layer 132 is a polycrystalline layer, and more particularly, polysilicon. For polysilicon formation, buffer layer 132 may be formed via a low pressure CVD at a temperature of 650°C. Plasma enhanced or photo enhanced CVD may also be employed for the formation of a polysilicon buffer layer 132. As noted previously, such CVD methods are well known in the art and therefore not discussed herein. Buffer layer 132 can likewise comprise an amorphous silicon. For amorphous silicon formation, buffer layer 132 may be formed via a low pressure CVD at a low temperature of 550°C, or other suitable method known in the art. Still further, buffer layer can alternatively comprise a poly-germanium layer.

As indicated above, buffer layer 132 provides a relatively soft layer. Buffer layer 132 essentially replicates the diamond surface and has an initial thickness greater than 0.1μm to overcome the roughness of the diamond insulation layer surface. Buffer layer 132 is then planarized through chem.-mech. polishing to a desired thickness. In the alternate embodiment, the planarized thickness of buffer layer 132 is in the range of 0.250 μm to 0.1 μm.

Subsequent to the formation of buffer layer 132, a thin oxide layer 126b. is formed on a top surface thereof. Oxide layer 126b. has a thickness in the range of approximately 1-50 nm. Preferably, oxide layer 126b. comprises a silicon oxide layer, such as SiO_2, of 25 nm in thickness and is thermally grown in an oxygen ambient at approximately 800 °C. Alternatively, oxide layer 126b. may be pryolytically deposited upon buffer layer 132.

The alternate embodiment bonded wafer structure 100 thus comprises a first primary wafer 120 and a secondary handle wafer 122. Primary wafer 120 comprises a substrate 124 having a thin oxide layer 126a. formed on a bottom surface thereof. Second-

ary handle wafer 122 comprises a substrate 128 having an insulation layer 130 formed on a top surface thereof, wherein, insulation layer 130 preferably is a chemical vapor deposited (CVD) diamond layer having a thickness of 0.5μm. Buffer layer 132 is formed on the top surface of insulation layer 130 and, subsequently, thin oxide layer 126b. is formed on the top surface of buffer layer 132. Primary wafer 120 is bonded to secondary handle wafer 122 via a heat treatment, as discussed previously, such that oxide layers 126a. and 126b. bond forming a single oxide layer 126. Oxide layer 126 is relatively thin, having a thickness in the range of 25-100 nm in comparison to an oxide layer having a thickness of 500 nm. Preferably, oxide layer 126 comprises silicon dioxide and is approximately 50 nm in thickness.

The wafer structure 100 as shown in Fig. 5 can be further processed by a conventional sequence of grinding, lapping,wet etching, and chem.-mech. polishing to obtain wafer structure 100 as shown in Fig. 6. As noted earlier, grinding, lapping, wet etching and chem.-mech. polishing are all well known in the art and further discussion thereof is not provided herein. Substrate 124 may be thinned to a desired thickness according to the requirements of a particular device. For instance, substrate 124 can be thinned to a thickness on the order of 2μm.

The resultant wafer structure 100 of Fig. 6 is thus suitable for the formation of semiconductor devices in the substrate 124. Substrate 124 preferably comprises an original silicon substrate which is substantially free of lattice mismatch defects and other defects. Thus, wafer structure 100 provides a wafer structure having a buried insulation layer in combination with a substrate in which lattice mismatch defects are minimized. Additionally, the thermal expansion coefficient of the buried insulation layer is substantially matched to the thermal expansion coefficient of the substrate which provides highly efficient transfer of heat away from active semiconductor device areas. Still further, the presence of the insulation layer 130 comprising diamond film, in addition to the buffer layer 132 and thin oxide layer 126, minimizes undesirable capacitive effects.

In yet another alternate embodiment according to the invention, wafer structure 10 is well suited for the formation of isolation trenches (Figs. 7 and 8). In particular, wafer structure 10 provides a reactive ion etch (RIE) stop layer comprising oxide layer 26. Oxide layer 26 further provides protection to the underlying insulation layer 30. Forming of an isolation trench having thermally oxidized trench sidewalls would cause problems if formed directly in a diamond insulation layer. The procedure according to the yet another alternate embodiment of the present invention circumvents the oxidation of the diamond film insulation layer, which occurs above 700 °C. RIE is well known in the art and therefore only briefly discussed herein.

Referring now to Fig. 7, there is shown wafer structure 10 which is formed by using the method described with respect to Figs. 1-3 and in which a first step RIE etch of the isolation trench formation has been completed. The top surface of substrate 24, after being thinned to a desired thickness as previously discussed, is oxidized and then deposited with a layer of nitride, using standard techniques, to form composite film 34. This composite film 34 is used as a trench masking layer. Trench patterning is then carried out using a conventional lithographic process to define trench locations 36 and 38 via a patterned photoresist film (not shown). The film layer 34 is then opened by carbontetrafluoride (CF_4) plasma etching. After etching, the photoresist film is stripped. A HBr/Cl_2 plasma is then used to etch the substrate 24 and stop at the buried oxide layer 26. Sidewalls 40 comprising 40a. and 40b. are then formed. Formation of trench sidewalls 40a. can be accomplished via thermal oxidation. A combination of thermal oxidation and CVD SiO_2 deposition and etch can be used to form sidewall spacer 40b. Thus, first step preliminary trenches 36 and 38, as shown in Fig. 7, are formed.

A second step trench RIE etch of the isolation trench formation is then performed for cutting through oxide layer 26, the insulation layer 30, and 500-1000 nm below the insulation layer 30 as shown in Fig. 8. That is, the second step etch comprises etching oxide layer 26 using top nitride mask layer 34 as a mask. A selective etch of oxide to nitride must be used. This etch is well known in the art and is not described herein. Then, insulation layer 30 is opened using an O_2/Ar plasma. This process has infinitive etch selectivity to oxide, nitride and silicon and is also well known in the art. Finally, a HBr/Cl_2 plasma is used again to overetch into the silicon substrate 28 of handle wafer 22 about 10% of the total trench depth.

Upon completion of the second step RIE etch, trenches 36 and 38 is preferably coated with a thin CVD SiO_2 coating 42 and subsequently filled using borophosphosilicate doped glass (BPSG), borosilicate doped glass (BSG), or polysilicon, as a trench fill 44. Only non-oxidative ambients are used during the fill process, since an oxidative ambient would attack the diamond insulation layer. CVD deposition of the trench fill 44 is then performed such that the fill is closed at the top of each trench when completed. Any voids or crevices created during trench filling can be eliminated by subsequently reflowing the trench fill glass between 900 to 1000 °C for approximately 30 minutes in nitrogen. This results in filled trenches 36 and 38 as shown in Fig. 9. The structure 10 may then be planarized to a desired thickness in preparation for subsequent device fabrication (Fig. 10).

Other methods of completing the isolation trenches 36 and 38, subsequent to the secondary trench etch, may be employed. For instance, the method for forming a void free isolation pattern, as

described in US-A-4526631 and 4689656, incorporated herein by reference, may be used.

The advantage of the above described two step RIE process in conjunction with the wafer structure 10 of the present invention is the formation of a "good" oxide near both device junctions at the surfaces of layer 24, i.e., at the interface of silicon 24 and oxide 26. The two step RIE process further provides for a non-oxidizing process for forming a CVD oxide on the buried insulation layer 30, i.e., the buried CVD diamond film.

The above two step RIE process, as described with respect to wafer structure 10, is similarly applicable to wafer structure 100, with the following differences. Wafer structure 100, as formed by the method described with respect to Figures 4-6, is processed via a second step RIE etch which also cuts through buffer layer 132. In particular, the second step etch for structure 100 comprises etching oxide layer 126 using a top nitride mask layer, similar to that described with respect to structure 10, as a mask. A selective etch of oxide to nitride must be used. Polysilicon buffer layer 132 is then etched in a HBr/Cl_2 plasma. Then, diamond insulation layer 130 is opened using an O_2/Ar plasma. Finally, a HBr/Cl_2 plasma is used to overetch into silicon substrate 128 of handle wafer 122 about 10% of the total trench depth. Since the polysilicon buffer layer 132 is a semiconductive film, the trench must etch to cut through this layer in order to form a well-isolated structure.

Thus it has been shown that in order to reduce the heat build-up of ECL circuits on SOI structures, the thick thermal SiO_2 oxide layer (500 nm) positioned between the two silicon wafers of prior art wafer structures is replaced by a (5000 nm) CVD diamond layer. Such a CVD diamond layer has a three orders of magnitude higher thermal conductivity (18-20 W/cm K) than thermally grown SiO_2. The CVD diamond film further has a dielectric constant between 3 and 6 (depending on process) and a low dielectric resistivity between $1X10^{10}$ and $1X10^{16}$ ohm cm (depending on process). Still further, the diamond film has a better match of the thermal expansion coefficient ($18X10^{-7}$ C^{-1}) with silicon ($32X10^{-7}$ C^{-1}) than SiO_2 ($5X10^{-7}$ C^{-1}). Lastly, the wafer structure of the present invention provides a well suited structure for isolation trench formation.

Claims

1. A wafer structure upon which semiconductor devices may subsequently be formed, said structure comprising:
   a) a first wafer comprising a first substrate having a first thin oxide layer formed on a bottom surface of the first substrate, the first substrate further having a characteristic thermal expansion coefficient; and
   b) a second wafer comprising a second substrate having an insulation layer deposited on a top surface of the second substrate, the insulation layer having a characteristic thermal expansion coefficient substantially matched with the characteristic thermal expansion coefficient of the first substrate of said first wafer, the insulation layer further having high thermal conductivity, said second wafer further having a second thin oxide layer formed on a top surface of the insulation layer, the second thin oxide layer further being planarized to a desired thickness,
   wherein the first thin oxide layer of said first wafer is bonded to the second thin oxide layer of said second wafer.

2. The wafer structure of claim 1 wherein said second wafer comprises:
   a second substrate having (i) an insulation layer deposited on a top surface of the second substrate, the insulation layer having a characteristic thermal expansion coefficient substantially matched with the characteristic thermal expansion coefficient of the first substrate of said first wafer, the insulation layer further having a high thermal conductivity, (ii) a buffer layer formed on a top surface of the insulation layer, the buffer layer further being planarized to a predetermined thickness, and (iii) a second thin oxide layer formed on a top surface of the buffer layer.

3. A wafer structure according to claim 1, wherein:
   the first thin oxide layer of said first wafer comprises a thickness less than 0.05μm;
   the insulation layer of said second wafer comprises a thickness less than 1.0μm; and
   the second thin oxide layer of said second wafer comprises a thickness less than 0.05μm.

4. The wafer structure of claim 1, 2 or 3, wherein the substrate of said first wafer comprises a substrate thinned down to a predetermined thickness.

5. The wafer structure of claim 1, 2 or 3, wherein the first substrate of said first wafer comprises a silicon substrate.

6. The wafer structure of claim 1, 2 or 3, wherein the insulation layer of said second wafer comprises a diamond layer.

7. The wafer structure of claim 6, wherein the diamond layer comprises a CVD diamond film layer.

8. The wafer structure of claim 3, wherein the first thin oxide layer of said first wafer and the second

thin oxide layer of said second wafer comprise silicon oxide layers.

9. The wafer structure of claim 2, wherein the buffer layer of said second wafer comprises a polycrystalline layer.

10. The wafer structure of claim 9, wherein the polycrystalline layer comprises polysilicon.

11. The wafer structure of claim 11, wherein the buffer layer of said second wafer comprises amorphous silicon.

12. The wafer structure of claim 2, wherein the first thin oxide layer of said first wafer and the second thin oxide layer of said second wafer comprise silicon oxide.

13. A wafer structure according to claim 2, wherein:
the first thin oxide layer of said first wafer comprises a thickness less than 0.05μm;
the insulation layer of said second wafer comprises a thickness less than 1.0μm;
the buffer layer of said second wafer comprises a thickness less than 0.1μm; and
the second thin oxide layer of said second wafer comprises a thickness less than 0.05μm.

14. A method of producing a wafer structure upon which semiconductor devices may subsequently be formed, said method comprising the steps of:
a) forming a first thin oxide layer on a bottom surface of a first substrate, the first substrate having a characteristic thermal expansion coefficient;
b) depositing an insulation layer on a top surface of a second substrate, the insulation layer having a characteristic thermal expansion coefficient substantially matched with the characteristic thermal expansion coefficient of the first substrate,
c) forming a second thin oxide layer on a top surface of the insulation layer and planarizing the second thin oxide layer to a predetermined thickness; and
d) bonding the first thin oxide layer to the second thin oxide layer.

15. The method of claim 14 wherein said insulation layer further has a high thermal conductivity.

16. The method of claim 14 or 15 wherein step c) consists of:
c1) forming a buffer layer on a top surface of the insulation layer and planarizing the buffer layer to a desired thickness; and,
c2) forming a second thin oxide layer on a top surface of the buffer layer.

17. The method of claim 14, 15 or 16, further comprising the step of:
e) thinning the first substrate of said first wafer down to a desired thickness.

18. The method of claim 14, 15 or 16, wherein said step of forming a first thin oxide layer on a first substrate comprises forming the first thin oxide layer on a silicon substrate.

19. The method of claim 14, 15 or 16, wherein said step of depositing an insulation layer comprises depositing diamond.

20. The method claim 19, wherein depositing diamond comprises depositing CVD diamond.

21. The method of claim 14 or 15, wherein:
said step of forming a first thin oxide layer comprises forming silicon oxide; and
said step of forming a second thin oxide layer comprises forming silicon oxide.

22. The method of claim 14 or 15, further wherein:
said step of forming a first thin oxide layer comprises forming a first thin oxide layer of a thickness less than 0.05μm;
said step of depositing an insulation layer comprises depositing an insulation layer of a thickness less than 1.0μm; and
said step of forming a second thin oxide layer comprises forming a second thin oxide layer of a thickness less than 0.05μm.

23. The method of to claim 16, wherein said step of forming a buffer layer comprises depositing a polycrystalline layer.

24. The method of to claim 23, wherein depositing the polycrystalline layer comprises depositing polysilicon.

25. The method of claim 16, wherein said step of forming a buffer layer comprises depositing amorphous silicon.

26. The method of claim 16, wherein:
said step of forming a first thin oxide layer comprises forming silicon oxide; and
said step of forming a second thin oxide layer comprises forming silicon oxide.

27. The method of claim 16, further wherein:
said step of forming a first thin oxide layer comprises forming a first thin oxide layer of a thickness less than 0.05μm;

said step of depositing an insulation layer comprises depositing an insulation layer of a thickness less than 1.0μm;
said step of forming a buffer layer comprises forming a buffer layer of a thickness less than 0.1μm; and
said step of forming a second thin oxide layer comprises forming a second thin oxide layer of a thickness less than 0.05μm.

FIG. 1

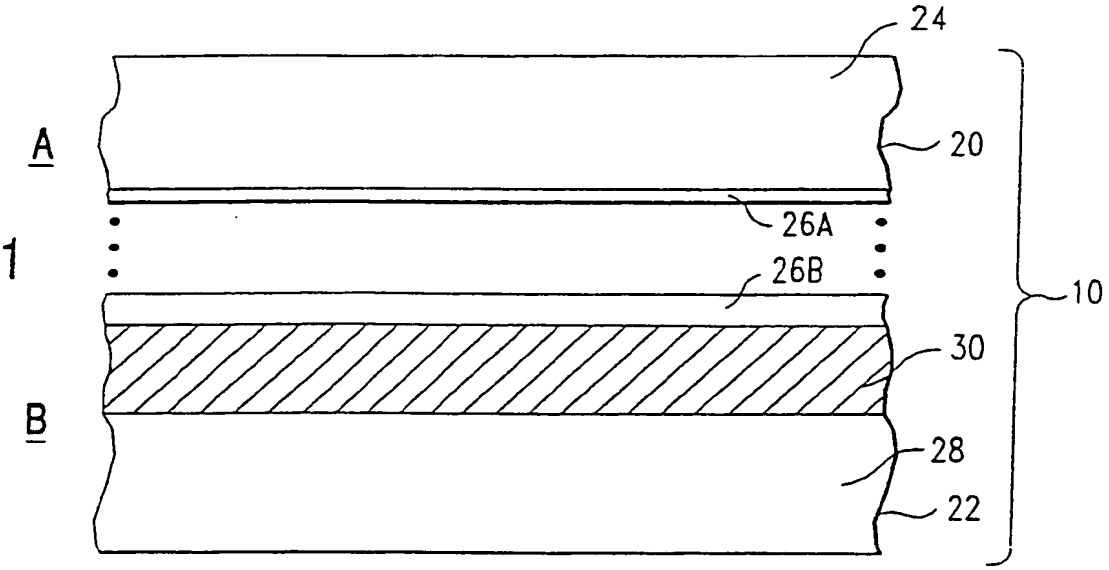


FIG. 2

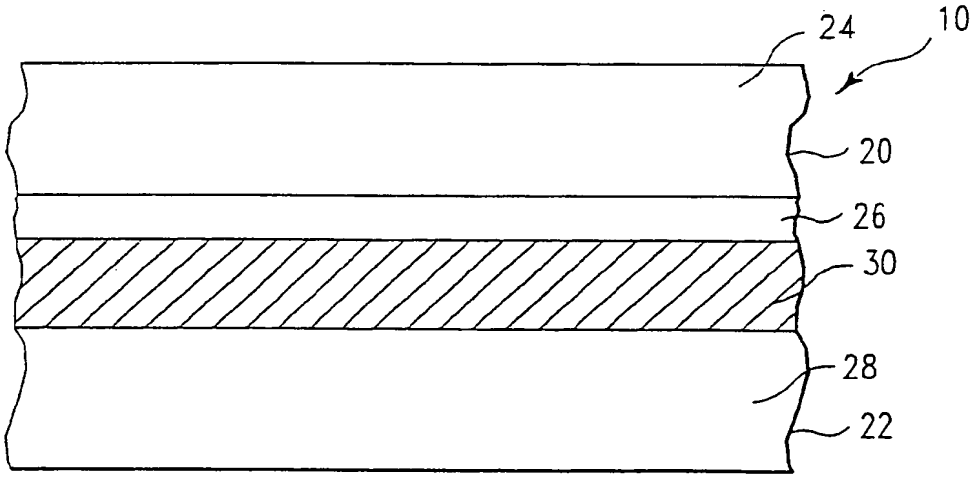


FIG. 3

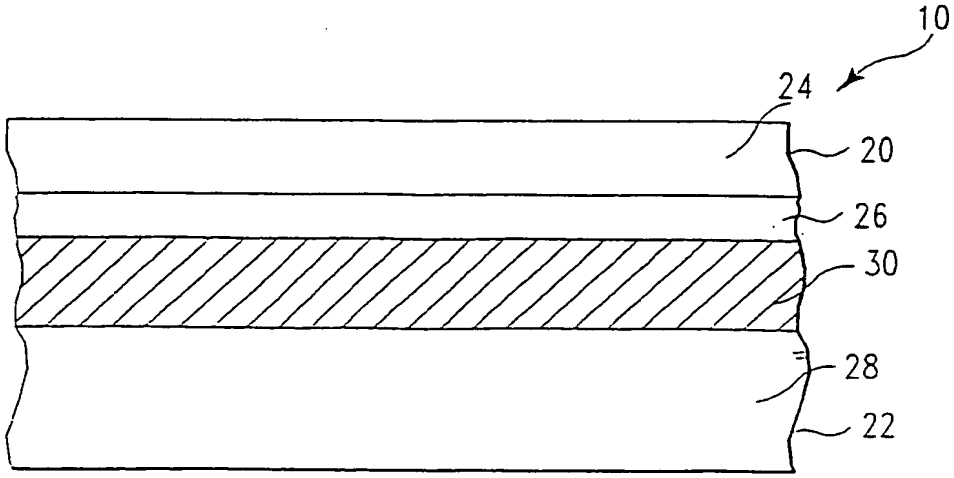


FIG. 4

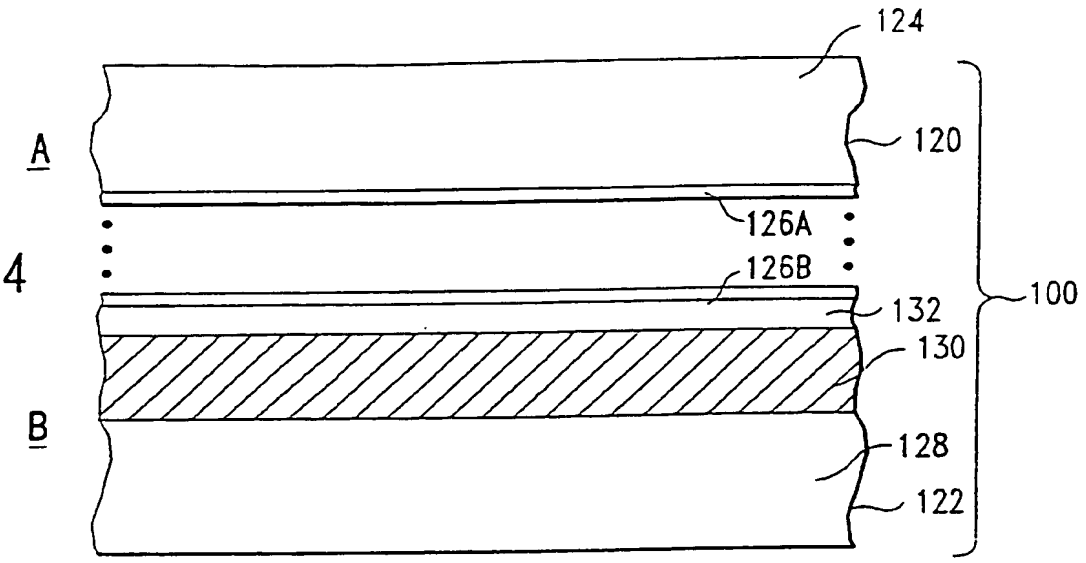


FIG. 5

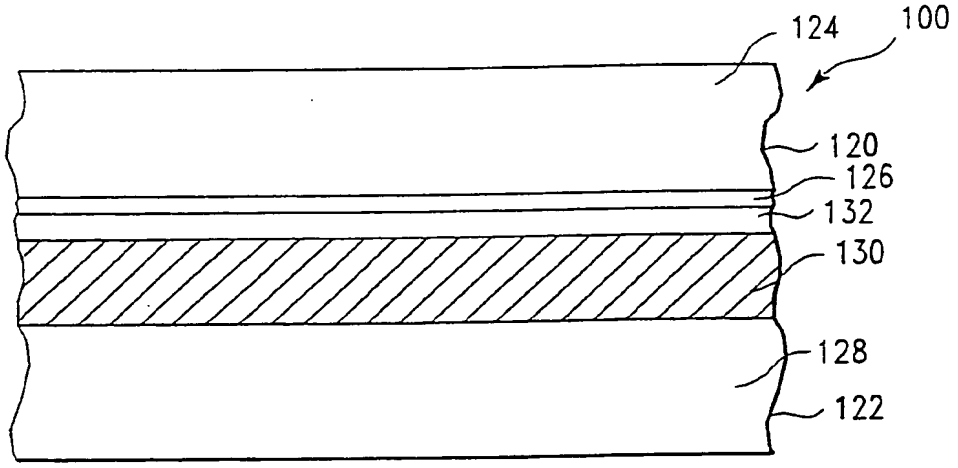
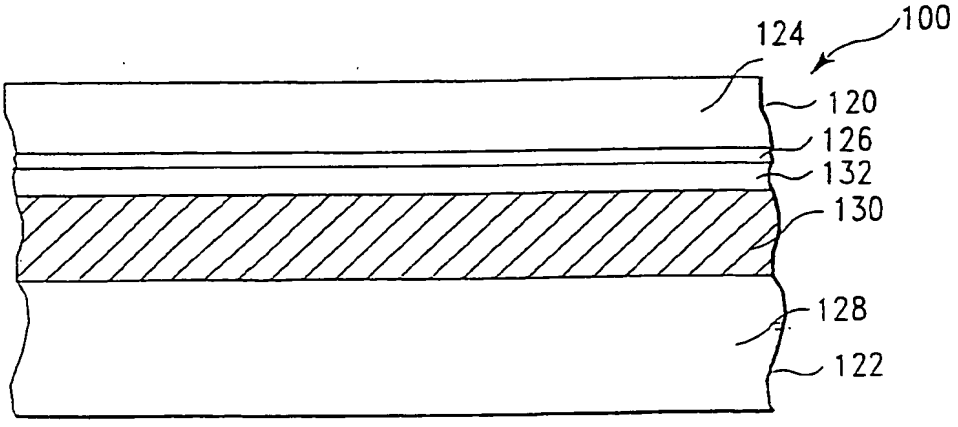


FIG. 6



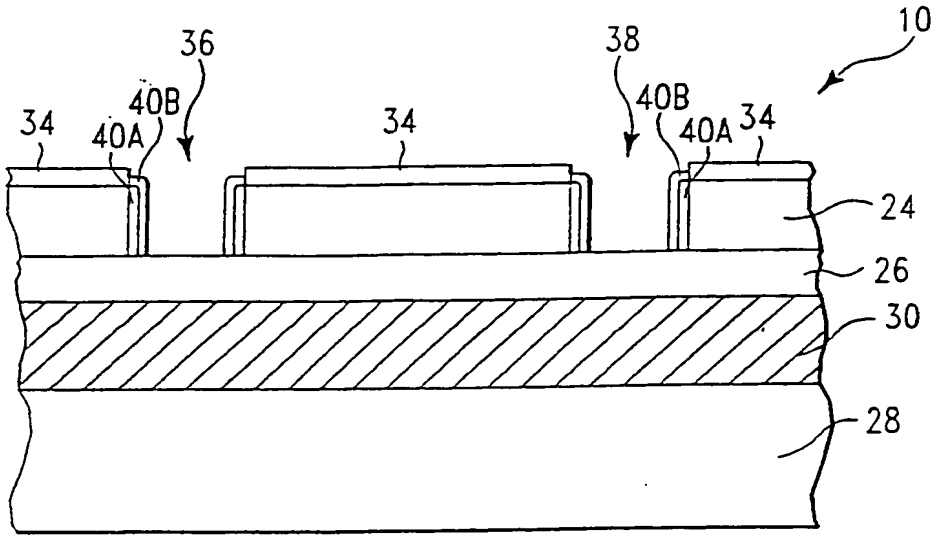


FIG. 7

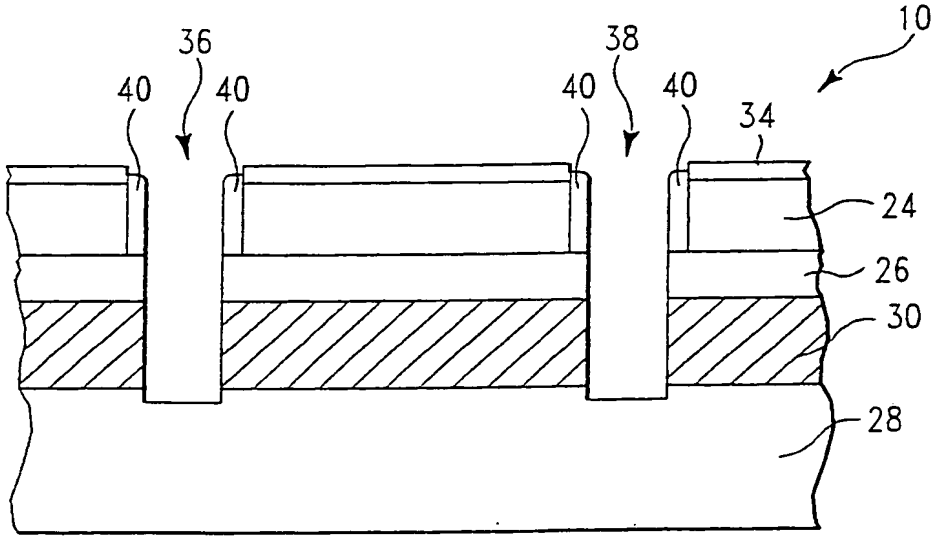


FIG. 8

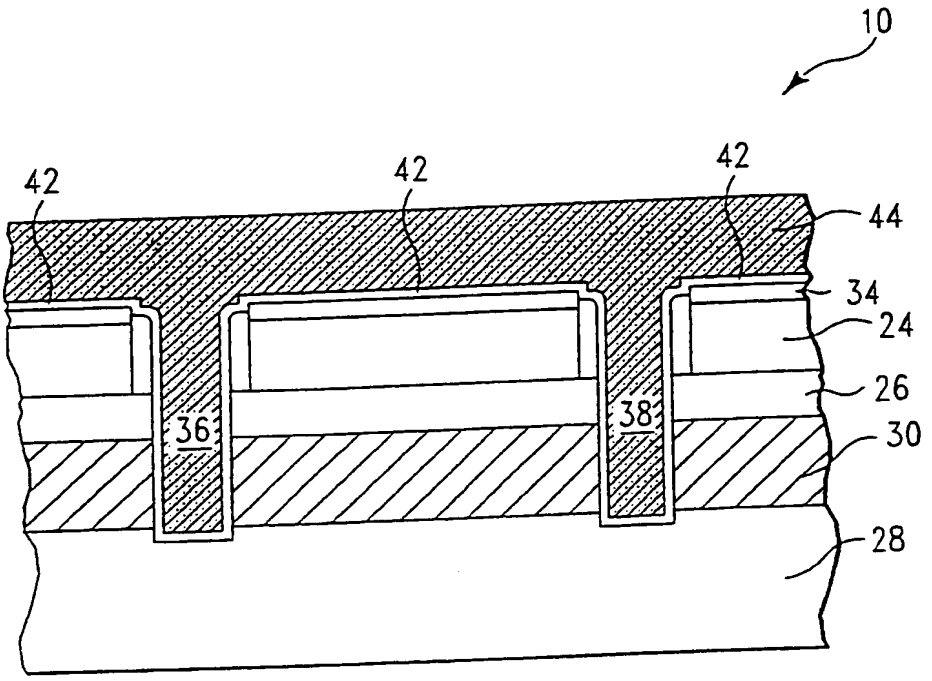


FIG. 9

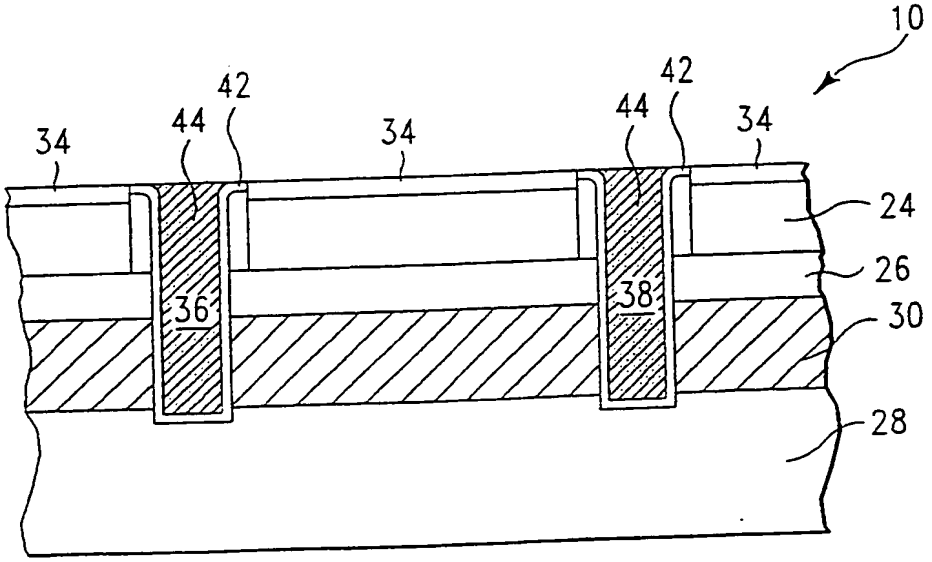


FIG. 10

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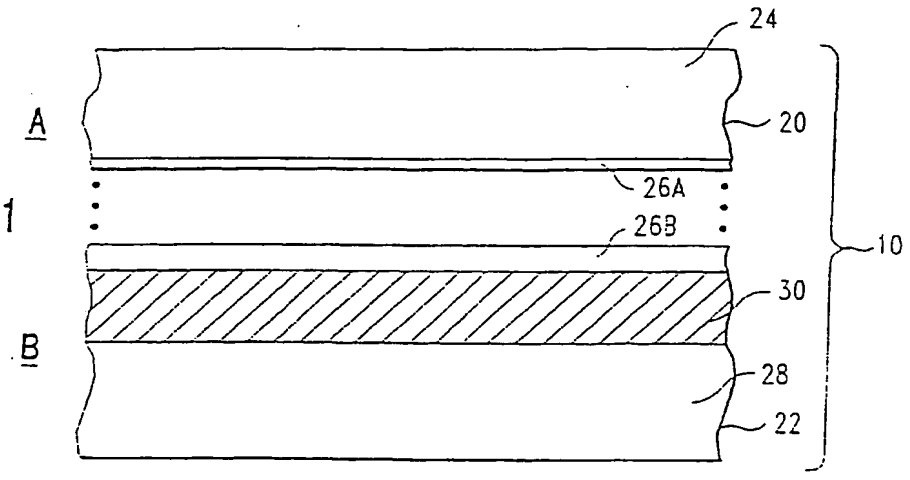
(54) Bonded wafer structure having a buried insulator layer

(57) A wafer structure and a method of making the same, upon which semiconductor devices may be formed, comprises first and second wafers. The first wafer (20) comprises a first substrate (24) having a thin oxide layer (26a) formed on a bottom surface thereof; the said first substrate having a characteristic thermal expansion coefficient. The second wafer (22) comprises a second substrate (28) having an insulation layer (30) formed on a top surface thereof, the insulation layer having a characteristic thermal expansion coefficient substantially matched with the characteristic thermal expansion coefficient of the first substrate and further having a high thermal conductivity. The second wafer further comprises a thin oxide layer (26b) formed on a top surface of the insulation layer, wherein the first thin oxide layer of the first wafer is bonded to the second thin oxide layer of the second wafer, to form a typical bonded wafer structure (10) that can be advantageously used in the fabrication of high speed high density integrated circuits.

FIG. 1



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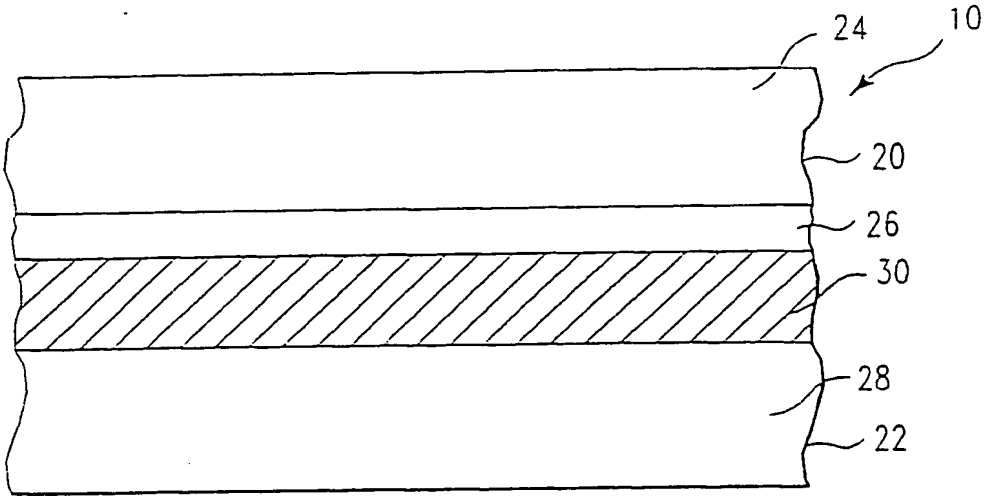
(Cont. next page)

FIG. 2



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EUROPEAN SEARCH REPORT

Application Number
EP 93 48 0044

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	WO-A-91 11822 (ASEA BROWN BOVERI) * claims 1-9; figure 2F * ---	1-27	H01L21/76 H01L21/20
A	WO-A-87 06060 (FAIRCHILD SEMICONDUCTOR CORP.) * page 5, line 28 - line 37; claims 1,3-6,12-16,23,24; figures 1A-1D * ---	1,4-7, 14,15, 18-20, 22,27	
A	EP-A-0 413 547 (SHIN-ETSU HANDOTAI CY) * claim 1; figure 1A * -----	1,3-5,8, 13,14, 17,18	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 January 1997	Vancraeynest, F

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